Hardware Configuration and Definition for z/OS

Day 1

Unit 1: HCD introduction

Unit 2: IOCP and MVSCP macro review

Unit 3: HCD dialog

Unit 4: LPAR and logical control unit concepts

Unit 5: OSAs, OSA/ICC and HiperSockets

Unit 6: Review of zSeries hardware

Exercise 1: Overview of lab environment

Exercise 2: HCD familiarity

Day 2

Unit 7: zSeries I/O architecture: Logical channel subsystems

Unit 8: Advanced DASD concepts: EAV/PAV and multiple subchannel sets

Unit 9: FICON, FICON CTCs, and FICON directors

Exercise 3: Coding a zSeries 2817

Exercise 4: Adding FICON directors to your configuration (optional)

Exercise 5: Incremental migration from IOCP deck (optional)

Day 3

Unit 10: HCD implementation and migration

Unit 11: IPL and LOADxx member

Unit 12: Dynamic I/O reconfiguration

Unit 13: z196 HCD and using CMT

Exercise 6: Building a LOADxx member

Exercise 7: Perform dynamic I/O

Day 4

Unit 14: FICON CTCs for sysplex

Unit 15: HCD and Parallel Sysplex

Exercise 8: Coding a 2817 using the CMT

Exercise 9: Coding CF coupling links

Exercise 10: Coding sysplex FICON CTCs